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Abstract
Nowadays the development of semiconductor industrial is very fast, and the technology enters to nanometer generation at present. Since the critical dimension (CD) in the advanced technology is smaller than the wavelength and the diffraction may cause pattern distortion problem on wafers. We call that is Optical Proximity Effect (OPE). It possibly causes that the lithography of layout patterns to wafers have the line width errors and also result in chip's yield reduction.
In this thesis, we present a new structure of the low power dynamic programmable logic array (DPLA). We also propose a DPLA compiler considering OPE to automatically generate DPLA layout. There are two methods to alleviate OPE problem for DPLA. First, we use the product line reordering algorithm to pre-arrange the order of product lines in a DPLA that can efficiently reduce OPE. Second, we have referred to many layout styles and concluded some design styles which have the lower OPE for DPLAs.
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